INTERUPTS IN INTEL 8085

The Intel 8085 microprocessor supports five interrupt signals. These interrupts are used to handle external events or conditions that require immediate attention by the microprocessor. The interrupts in the Intel 8085 are as follows:

1. TRAP: It is a non-maskable interrupt (NMI) and has the highest priority among all interrupts. It is generally used for critical error conditions or emergencies that require immediate attention. The TRAP interrupt cannot be disabled or masked.
2. RST 7.5: This is a maskable interrupt and has the second-highest priority. It is often used for system restart or initialization routines.
3. RST 6.5: Similar to RST 7.5, this is also a maskable interrupt but with a lower priority. It can be used for general-purpose interrupt handling.
4. RST 5.5: Another maskable interrupt with lower priority than RST 6.5. It can be used for various purposes, depending on the specific application.
5. INTR: This is a maskable interrupt and has the lowest priority among all interrupts. It is usually used for external devices or peripherals to request service from the microprocessor.

To handle interrupts, the Intel 8085 provides an interrupt enable flip-flop (IFF) and an interrupt enable (IE) flag. The IFF is a two-bit register that stores the current state of interrupt enable and the previous state of the interrupt enable. The IE flag is set or cleared by the programmer to enable or disable interrupts. When an interrupt occurs, the microprocessor checks the state of the IFF and the IE flag to determine whether to service the interrupt or not.